UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,866	01/05/2004	Yoshitaka Mano	60188-741	3236

7590 08/10/2005

Jack Q. Lever, Jr.
McDERMOTT, WILL & EMERY
600 Thirteenth, N.W.
Washington, DC 20005-3096

EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,866	MANO ET AL.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4-13* is/are allowed.

6)☒ Claim(s) *14 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *May 4, 2005*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *08012005*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment/IDS

The amendment submitted on May 24, 2005, and the IDS submitted on May 4, 2005, have been reviewed and considered with the following results:

The new title, and the amended paragraph have overcome their respective objections described in the previous Office Action. Therefore, they have been withdrawn.

The cancellation of claims 1-3 rendered their objections and rejections moot.

The amended claims overcame the objections of claims 4-13, and the rejections of claims 9-13 under 35 U.S.C. 103(a) with respect to the applicant's own Prior Art Fig. 8 and Kwan. These references do not clearly show or disclose a load circuit, connected to the switching transistor, having a first resistor and a load adjustment section as recited within the claim. Therefore, those objections and rejections from the previous Office Action have all been withdrawn.

However, when reviewing the claims, including the newly added claims, several concerns were noted. The objections to claims 5, 10, and 12, described later under the appropriate section, were inadvertently overlooked by the examiner (i.e. were not described in the previous Office Action). Also, newly added claims 15-16 have rejections described later under the appropriate section.

Although the applicant's representative Alex Chan (Reg. No. 52,713) was originally contacted on Aug 1, 2005 to discuss the above concerns for a possible Examiner's Amendment if suitable wording could be agreed upon. However, the examiner learned on Aug 5th that the

applicants would not be available for a response until Aug. 19th. Therefore, this action is being submitted, thus providing the applicants time to respond.

The references cited on the recent IDS do not clearly show or disclose all the limitations recited within the claims. U.S. Patent 5,202,838 (corresponding to JP 04-032988) shows a circuit that control voltage applied to internal circuit 17, with its outputs controlling parallel current paths, each comprising a switching transistor and some type of load device. However, it is not clear if the current flowing within internal circuit 17 will be substantially the same as the current flowing within these parallel current paths. Also, the reference does not clearly show a load adjustment section. For example, if only one switching transistor (e.g. 18) and its load circuit (e.g. 19) are considered, it has no adjustment section. In U.S. Patent 6,343,022 (corresponding to JP 2001-101364), the relationships between the internal circuit, switching transistor, and current within the load circuit are not the same as those recited within the present application's claims. For example, although the reference discloses 49 (50, 51) consumes the same amount of current as 46 (47, 48) in the operation mode, if any one of circuits 46-48 is deemed the internal circuit of Fig. 12, its output does not control its corresponding switch (53, 55, or 57). If block 18 is considered the internal circuit, the relationships between the amounts of current flowing within 18 and 49-51 are not clear because 49-51 have the same current consumption as 46-48, but circuit 43 will also consume current, and that is not disclosed. Therefore, the present application's amended claims are deemed patentably distinct over these references.

Claim Objections

Claims 5, 10, and 12 are objected to because of the following informalities: Claim 5, line 4 should have "an" replaced by --the-- since "an operational period" is already recited on line 10 of claim 4. Line 2 of both claims 10 and 12 should have "a drain" changed to --the drain--, wherein the drain was previously identified on line 8 of claim 4. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 14-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. The last two lines of claim 14 are not clear with respect to how the adjustment of the current consumed by the load circuit relates to the current consumed by the internal circuit (e.g. see lines 7-9 of the claim wherein the load circuit current is "substantially the same amount of electric current which the internal circuit consumes"). For example, if the load circuit's current is adjusted, is the current consumed by the internal circuit also adjusted? It is suggested --when the switching transistor is ON-- be added after "consumes" on the last line of claim 14. This will more clearly indicate that the current adjustment would occur when the switching transistor is on, thus allowing the current to flow through the load circuit. It appears the "more than the amount of electric current" in lines 3-4 of claim 15 can contradict claim 14's "substantially the same amount" limitation. Therefore, the following changes to claim 15 are suggested: 1) add --and if-- prior to the first occurrence of "the amount" on line 3; 2) change

"an" to --the-- on line 4 to relate back to the "operation period" in claim 14; 3) add --adjusted to be-- after "is" on line 6; and 4) replace "when the fuse device is cut" on line 7 with --by cutting the fuse device--. These changes will help relate the current type limitations of claim 15 to those already recited within claim 14 by further clarifying the current adjustment.

Claim 15 recites the limitation "the first resistor" in line 3. Since there is insufficient antecedent basis for this limitation in the claim, it is suggested --a first resistor,-- be added after "includes" on line 13 of claim 14. This change will provide a proper antecedent basis for "the first resistor" within claim 15, and help the claimed limitations read over the prior art.

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. (Takahashi), in view of Kwan, wherein both of these references were cited in the previous Office

Action. Fig. 6 of Takahashi shows internal voltage supply circuit 10 generating internal voltage VINT; internal circuit 1 operated by internal voltage VINT; switching transistor 33 receiving operating signal PA at its gate; and load circuit 43,42 connected to the drain of switching transistor 33. Since internal circuit 1 and block 40 are coupled in parallel between VINT and ground, one of ordinary skill in the art would understand that when internal circuit 1 is in operation, current I0 will substantially flow through that circuit, and when internal circuit 1 is not in operation, current I0 will substantially flow through 33 and 43 within block 40. Therefore, it is understood their currents will be substantially the same, with respect to when the current flows through them. Fig. 6 also shows load circuit 43,42 comprising load adjustment section 43,42 that allows for current adjustment through load circuit 43,42. However, the reference shows/discloses the operation of both switching transistor 33 and internal circuit 1 is based on the ACTIVE SIGNAL, instead of the switching transistor receiving operation signal PA from internal circuit 1. Fig. 1 of Kwan shows internal circuit 103 and dummy load 101 coupled in parallel, wherein load 101 receives operational signal 102 from internal circuit 103. Kwan's Figs. 2C and 2D each show dummy load 101 comprising switching transistor receiving at its gate an operation signal (e.g. NMC) from internal circuit 103, and load circuit R connected to the drain of the switching transistor. One of ordinary skill in the art would understand the relationships between the currents within 103 and 101 (e.g. as described on column 5, lines 4-13, and 26-38), closely correspond with Takahashi's relationships between internal circuit 1 and block 40. Therefore, it would have been obvious to one of ordinary skill in the art to apply the teachings disclosed by, and understood from, Kwan to the circuitry of Takahashi. In this case, Takahashi's ACTIVE SIGNAL can be applied only to internal circuit 1 to determine its

operational state, and an output of internal circuit 1 can be used to control switching transistor 33, thus rendering claim 14 obvious. By being controlled directly from internal circuit 1, block 40 will provide corresponding operation related directly to the operational state of internal circuit 1. Otherwise, if internal circuit 1 has a slower or faster response time to ACTIVE SIGNAL than block 40, block 40 could operate at an inappropriate time (e.g. it could allow some of current I0 to flow through block 40 when all the current should flow into internal circuit 1).

Claims 1-3 have been cancelled.

Allowable Subject Matter

Claims 4-13 are allowed. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure the semiconductor device comprises a switching device, and the load circuit with a first resistor and load adjustment section, as recited within independent claims 4 (upon which claims 5-12 depend) and 13. However, it is suggested the minor objections to claims 5, 10, and 12 be addressed/corrected.

Claim 15 would be allowable if satisfactorily rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. There is also no strong motivation to modify or combine any prior art reference(s) to ensure the load circuit includes first/second resistors, and the fuse device as claim 15 recites. However, the problems related to the "the first resistor" and the amount of current consumption must first be clarified within claim 15.

THIS ACTION IS MADE FINAL. The applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund
8 August 2005

MY-TRANG NUTON
PRIMARY EXAMINER
8/8/05